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EXAMINER	
RIZZUTO, KEVIN P	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/683,351	LEBER ET AL.	
	Examiner	Art Unit	
	Kevin P Rizzuto	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2002 and 17 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☒ Claim(s) *1-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/17/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-10 have been examined.

2. Acknowledgement of papers filed: Declaration or oath on 3/12/02, priority papers on 03/12/02 and the Information Disclosure Statement on 7/17/03. The papers filed have been placed on record.

Priority

3. Receipt of papers submitted under 35 U.S.C. 19(a)-(d) is acknowledged, the certified copy of German Application 00128490.0, filed on 12/23/2000 has been received and placed on record.

Drawings

4. Figure 11 is objected to for minor informalities. A flow chart is shown that does not have all the boxes connected as the specification describes it. Boxes 1130, 1140, 1170, 1180, 1190 and 1195 appear to be missing connections such as arrows to disclose the steps that are taken.

5. Figures 1, 2, 3, 4 and 5 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

6. Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action n to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective

action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

7. The disclosure is objected to because of the following informalities: Incorrect grammar in multiple instances of the word bit, for example paragraph 38, "32-bit" of the result" should be "32-bits". Also, paragraph 40, "all 64 bit need" should be "all 64 bits need."

Appropriate correction is required of these and any other instances of such errors.

Claim Objections

8. Claims 1-10 are objected to because of the following informalities: The term "bitlength" is used. In proper English, "bitlength" should be written as two words or hyphenated. Appropriate correction is required.

9. Claim 1 is also objected to because "the target register" of line 6 lacks antecedent basis. "The target register" will be interpreted as "a target register" for the remainder of the examination. Appropriate correction is required.

10. Claim 5 is objected to because of the following informalities: Applicant claims, "said second instruction," which lacks antecedent basis. "Said second instruction" will be interpreted as "a second instruction" for the remainder of the examination. Appropriate correction is required.

11. Claims 8, 9 and 10 are objected to because of the following informalities. A "so_extract" instruction is added and is then later referred to as "said extract" instruction. This is inconsistent language and the "said extract" lacks antecedent basis.

Claim Rejections - 35 USC § 112

12. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

13. Claims 1-10 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

14. As per claim 1, 2, 8, 9 and 10, where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The term "result field" in claim 1 is used by the claim to mean the physical or logical result/destination/target register, while the accepted meaning is a set of bits that act as an address to specify the destination register. The physical or logical destination register gets the result of the operation, not the field in the instruction that specifies the destination register. Patterson and Hennessy discuss this in pages 118 and 119.

15. As per claim 1, applicant states, "adding a so-called 'extract' instruction." This is indefinite because it does not clearly state whether the instruction added is an "extract" instruction or not. It is recommended that the word "so-called" be removed. Also, in line 5, "a first smaller bitlength instruction" is detected, however, it is unclear whether the smaller bit length is referring to the size of the instruction or the size of the instruction result as is implied by the preamble of the claim. For the remainder of the examination, the smaller bit length instruction will be interpreted as an instruction that produces a smaller bit length result.

16. As per claims 3, 4, 5, 6 and 7, each is dependent on claim 1 and, therefore, also rejected under 35 U.S.C. 112, second paragraph.

17. As per claims 8, 9 and 10, "a first smaller bitlength instruction" is detected, however, it is unclear whether the smaller bit length is referring to the size of the instruction or the size of the instruction result as is implied by the preambles of the claims. For the remainder of the examination, the smaller bit length instruction will be interpreted as an instruction that produces a smaller bit length result.

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 1-5 and 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mahurin, U.S. Patent 6,493,819 in view of Isaman, U.S. Patent 6,449,710, and Superscalar Microprocessor Design by Johnson and Hennessy and Patterson, Computer Organization and Design.

20. As per claims 1, 8, 9 and 10 Mahurin teaches a method for operating a processor having an architecture of a larger bit-length with a program comprising instructions compiled to produce instruction results of at least one smaller bit-length, characterized by the steps of: (The x86 instruction set has instructions capable of producing larger and smaller results. For instance, instructions can produce results of 8, 16, or 32 bits to be stored in registers of 32 bits (Column 1, line 63 to column 2, line 21 and column 7, lines 27-35). Therefore the processor that executes x86 instructions has an architecture of a larger bit length (32 bits) and also produces results of varying sizing, including "smaller" bit lengths (Also stated in Column 4, lines 58-64).

-Detecting when in program order a first smaller bit-length instruction is to be dispatched which does not have the target register address as one of its sources (Mahurin teaches the detection of x86 instructions that update portions of registers in the MROM unit. Also the instructions are detected when they do not have the target address as its source (Column 5, lines 43-54 and column 10, lines 40-51).

-Adding a so-called "extract" operation into an instruction stream before the smaller bit-length instruction, the extract operation comprising the following steps of: (The MROM unit 34 adds a "read" (extract) operation into the instruction stream. A read of the destination register is done prior to the execution of the detected instruction. This

read is a function performed by the processor as a result of control signals. The operation is carried out before the execution of the detected instruction so it was added prior to the instruction in the instruction stream (Column 5, 35-54).).

a. Dispatching instructions from an instruction queue (MROM unit 34) into a Reservation Station (The MROM unit 34 conveys its instructions to the Decode Unit 20A, which in turn dispatches its instructions to the Reservation Station 22A. (Figure 1 and column 6, lines 24-52). Mahurin also teaches parallel dispatching to reservation stations. In figure 7 the multiple decode units all have the ability to dispatch instructions. Also, in column 7, line 62 to column 8, line 26 describes the multiple instruction issuing per cycle.)

b. Issuing instructions to an Instructional Execution Unit (IEU) as soon as all source operand data is available and an IEU is available according to respective issue scheme: (Reservation station 22A issues instructions to the execution unit (Functional unit 24A) Column 8, lines 27-46)

c. Executing instructions by an available IEU (column 8, lines 27-65)

d. Setting an indication that the result of said instruction needs to be written into the result register of the instruction following the extract instruction: (Dest Size signal 210 indicates to Select Logic to write the result of the read (extract) operation into the result register of the detected smaller instruction. Figure 3 and column 14, line 52 to column 15, line 21.)

e. Writing the extract instruction result into the result register of said first instruction, and into all registers of operands being dependent of said first instruction:

(The result of the read (extract) operation is merged with the results of the detected smaller instruction that only updates a portion of a register, and it is written into the destination register specified by the detected smaller instruction and the result is used by instructions that are dependent. Column 15, lines 14-40).

21. While Mahurin does teach that a read of the destination register is done before the execution of the detected smaller instruction after the MROM unit detects the smaller instruction that does not have a target register as a source register, Mahurin fails to teach that the read (extract) operation is a separate read instruction that is dispatched together with the following smaller bit-length instruction from an instruction queue into a reservation station, that the (read) extract instruction is issued to an Instructional Execution Unit (IEU) as soon as all source operand data is available and an IEU is available according to respective issue scheme, and that the read (extract) instruction is executed by an available IEU.

22. Isaman teaches the insertion of an extra microinstruction (one instruction slot away from the detected instruction) in order to handle an instruction that updates only a portion of a register. The microinstruction performs, among other things, an extraction of the data in destination register, and it is processed like a regular instruction (Figures 2 and 3). The microinstruction is dispatched to the issue shelf, issued to an available execution unit and executed (Column 17, lines 45-65).

23. It would have been obvious for one of ordinary skill in the art to recognize that an instruction that requires a read function to be carried out could be simplified by implementing a separate serialized read microinstruction that is inserted in an

instruction slot one away from the detected instruction. Mahurin teaches that the read is carried out prior to the execution of the detected smaller instruction. Mahurin teaches that the MROM unit 34 detects the smaller instructions that only update a portion of a register. The separate microinstruction could come from the MROM unit 34 and be processed like any other instruction (or microinstruction). Mahurin teaches that instructions detected by the MROM unit are broken into simpler instructions and output to the Decode Units 20A-C (Column 5, lines 35-42, Mahurin). They are then dispatched to the Reservation Stations 22A-C. They are then issued to the execution units after their requirements are met, which is explained in Column 8, lines 27-46 of Mahurin. The requirements for issuing that Mahurin lays out would require that the separate read microinstruction would have to be issued and executed prior to the smaller instruction. In turning the read operation into a separate instruction to be dispatched, issued, and executed, instead of concurrently doing the read while the detected smaller instruction is being processed, a hardware reduction can occur. A read of a register, and write to another register is done on many instructions in the x86 instruction set, therefore, the hardware needed to implement a read microinstruction is already present. Breaking down one complex instruction into multiple simpler instructions is well known in the art and is taught in Hennessy and Patterson, page 175 and is the intention of the MROM unit. The smaller instruction would only have to be detected once (in the MROM unit) and the reservation station would not need to implement its special issuing scheme (described in column 11, lines 21-33). The hardware could then be simplified and reduced in the reservation station.

24. The reduction and simplification of hardware would have provided the motivation to implement the read instruction of Mahurin in a separate microinstruction inserted into the instruction stream by the MROM unit 34.

25. Mahurin in view of Isaman does not teach the dispatching of the read instruction and the detected smaller instruction together to a reservation station. Mahurin does teach that multiple instructions are dispatched together, however it is to multiple reservation stations instead of one reservation station.

26. Johnson teaches a single reservation station (central window) that can have multiple instructions dispatched to it. A single reservation station is more efficient than multiple reservation stations because it holds all instructions for issue regardless of which functional units execute the instructions (page 133 of Johnson). It would have been obvious to combine the use of only one reservation station with the parallel dispatching of Mahurin, which would mean parallel dispatching to a single reservation station. When both instructions are decoded and known, and there is room in the reservation station, they would be dispatched together, the read instruction to be executed first and the detected instruction executed after. By implementing only one reservation station, the multiple dispatching of instructions that are in order (column 6, lines 24-38 of Mahurin) would cause the read instruction and the detected smaller instruction to be dispatched together to a reservation station, since they are back to back as taught in figure 2 of Isaman.

27. Reducing the number of reservation stations to one would have allowed the instructions to be dispatched together to a reservation station. The increased efficiency of one reservation station would have provided the motivation to do the reduction.

28. As per claim 2, Mahurin, in view of Isaman and, teaches the method according to claim 1 including the step of writing the extract instruction result into the result field of said first instruction. It is taught that the extract and detected smaller instruction are one after the other sequentially. It is also taught that a reservation station addresses registers for instructions by tag addresses (Column 7, lines 36-61 of Mahurin). However, Mahurin, in view of Isaman and Johnson, is silent on how the writing of the result of the extract instruction is controlled. Hennessy and Patterson teach a program counter in which the next sequential address is determined by incrementing it (Page 384). A tag specifies a location and therefore is just another term for an address.

29. It would have been obvious to one of ordinary skill in the art that when the two sequential instructions are dispatched, as taught above, where the first read (extract) instruction must write to the destination register of the instruction following it (smaller detected instruction), the tag should be incremented to whatever the tag specifying the destination register is. This is the same as the program counter of Hennessy and Patterson being incremented by whatever value is necessary to get to the next sequential instruction. Incrementing a program counter to get a new address value is used by modern processors and therefore incrementing the value of a tag (address) is very well known in the art. Using a well-known method in order to allow two instructions writing to the same renamed register would make the design of the processor simpler

and easier. This would have provided the motivation to combine the incrementing method of the program counter of Hennessey and Patterson with Mahurin in view of Isaman and Johnson.

30. As per claim 3, Mahurin, in view of Isaman and Johnson, teaches the method according to claim 1, and also teaches having the larger bit length equal to 32 bits and having a smaller bit length equal to 16 bits.

31. Mahurin fails to teach that the larger bit length is 64-bits and the smaller bit length is 32-bits.

32. It would have been obvious for Mahurin to have a larger bit length of 64-bits and a smaller bit length of 32-bits because more data can be stored in registers of those sizes than the current register sizes. This would allow more precise values to be stored in a single register and allow more data overall to be present inside a register file with the same size bus for addressing registers.

33. It also would have been obvious to one of ordinary skill in the art at the time the invention was made to implement Mahurin's invention on a larger bit length equal to 64-bits and a smaller bit length equal to 32-bits since it has been held that changes in size that have no unexpected results is obvious. In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955).

34. As per claim 4, Mahurin, in view of Isaman and Johnson, teaches the method according to claim 1, and also teaches having the larger bit length equal to 32 bits and having a smaller bit length equal to 16 bits.

35. Mahurin fails to teach that the larger bit length is 128-bits and the smaller bit length is 64 or 32-bits.

36. It would have been obvious for Mahurin to have a larger bit length of 128-bits and a smaller bit length of 64 or 32-bits because more data can be stored in registers of those sizes than the current register sizes. This would allow more precise values to be stored in a single register and allow more data overall to be present inside a register file with the same size bus for addressing registers.

37. It also would have been obvious to one of ordinary skill in the art at the time the invention was made to implement Mahurin's invention on a larger bit length equal to 128-bits and a smaller bit length equal to 64 or 32-bits since it has been held that changes in size that have no unexpected results is obvious. In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955).

38. As per claim 5, Mahurin, in view of Isaman and Johnson, teaches the method according to claim 1, further comprising the step of when said second instruction is dependent of the first instruction, selectively inserting an extract instruction: (Mahurin teaches the selective insertion of extract instructions depending on if the result of an instruction updates only a portion of a register or not (Column 5, lines 43-54). This selective insertion occurs for all instructions going through the MROM unit 34, including when a second instruction is dependent on the detected first instruction.)

39. As per claim 7, Mahurin, in view of Isaman and Johnson, teaches the method according to claim 1, further comprising the step of associating the same instruction execution unit for said first and said extract instruction: (Figure 3, the results of the read

taught by Mahurin and the detected first instruction are both associated with the same (IEU) functional unit 24A. Mahurin teaches one functional unit is used with both of their instruction results, which shows the two instructions are associated with the same functional unit by means of their results).

40. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mahurin, U.S. Patent 6,493,819 in view of Isaman, U.S. Patent 6,449,710 and Superscalar Microprocessor Design by Johnson as applied to claim 1 above and further in view of White, U.S. Patent 5,74,928, Gover, U.S. Patent 5,752,062 and Hennessy and Patterson, Computer Organization and Design.

41. As per claim 6, Mahurin, in view of Isaman and Johnson, teaches the method according to claim 1, including the dispatch of multiple instructions per cycle to a reservation station and also the results of the read (extract) and first detected instruction are combined (reducing the respective multiple input signals for the latch) in the functional Unit 24A by multiplexors as shown in figure 3, but is silent on what logic blocks are used to build the multiplexor and is also silent on further teaching the steps of:

Dispatching said first instruction in the same cycle as the extract instruction and assuring that in the same cycle both or none of said two instructions is written into a reservation station means

-And fails to teach in case of a multiple write into the same result latch reducing the respective multiple input signals for the latch by either one of an OR gate or an AND gate, respectively.

42. White teaches an instruction that is broken down into two microinstructions, the first microinstruction being for reading an operand out of the register file. The two microinstructions are dispatched together in the same cycle, or not dispatched at all, because they are both in the same dispatch window (Column 7, lines 16 to column 8, 16). They are also both dispatched to the same reservations station (floating point reservation station 44, figure 14 and column 12, lines 5-56).

43. It would have been obvious to one of ordinary skill in the art to dispatch the two instructions together in the same cycle as taught by White. The two instructions of White are dispatched simultaneously in order to process the two instructions as quickly as possible. Parallelizing steps in a processor is a well-known method in the art to increase processing speed. This is desirable in many instructions, especially instructions such as loads, in which other instructions are usually dependent and a stall or hazard causes large or many delays (Grover, column 15, lines 6-35). Dispatching them both to a reservation station simultaneously will ensure that once the read of the specified destination register is executed, the detected smaller instruction will already be in the reservation station and ready to be issued. The improved processing by avoiding load stalls would have provided the motivation for combining Mahurin and White.

44. In case of a multiple write into the same result latch reducing the respective multiple input signals for the latch by either one of an OR gate or an AND gate, respectively, Hennessy and Patterson show on page B-9 that a multiplexor is commonly made using AND with OR gates.

45. It would have been obvious to one of ordinary skill in the art to use AND and OR gates to implement the multiplexor of Mahurin because it is well known in the art as a method to implement a multiplexor. One of ordinary skill in the art would have recognized that a basic, simple method to implement a multiplexor is using AND and OR gates, because it is taught in numerous text books including Hennessy and Patterson in the section titled "The Basics of Logic Design." The simplicity of creating a multilplexor out of AND and OR gates would have provided the motivation to do so.

Conclusion

46. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

47. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin P Rizzuto whose telephone number is (571)272-4174. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571)272-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KPR

RICHARD L. ELLIS
PRIMARY EXAMINER